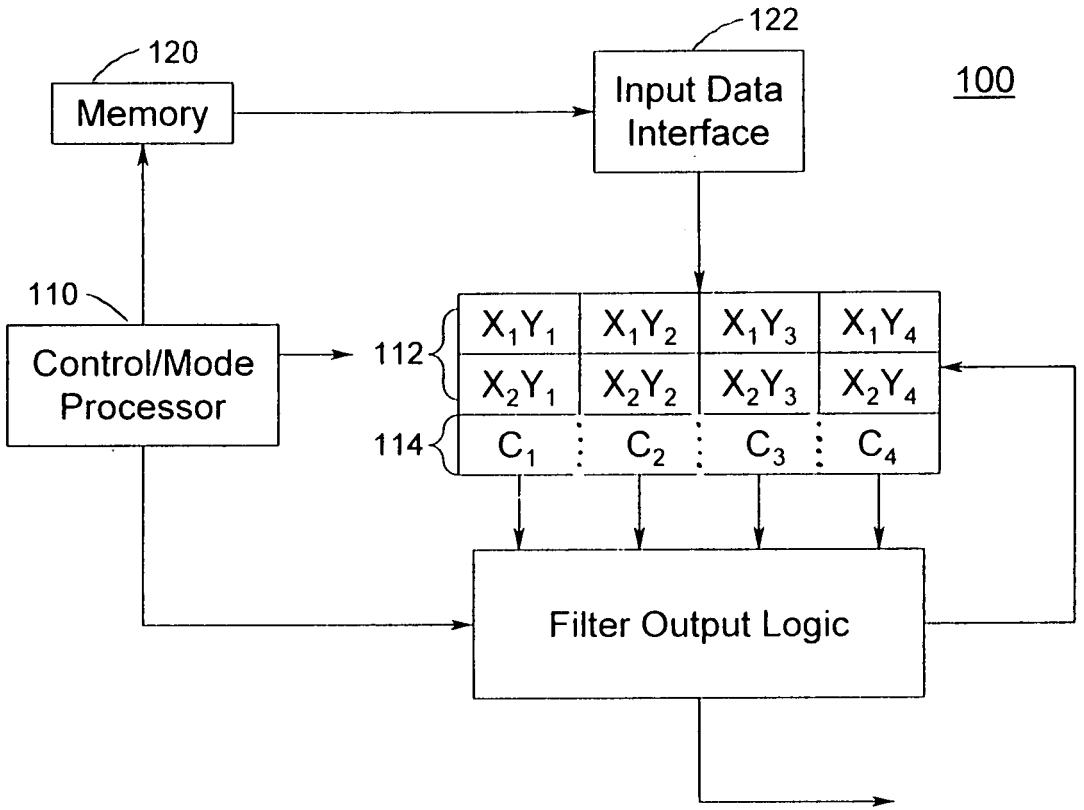


FIG. 1

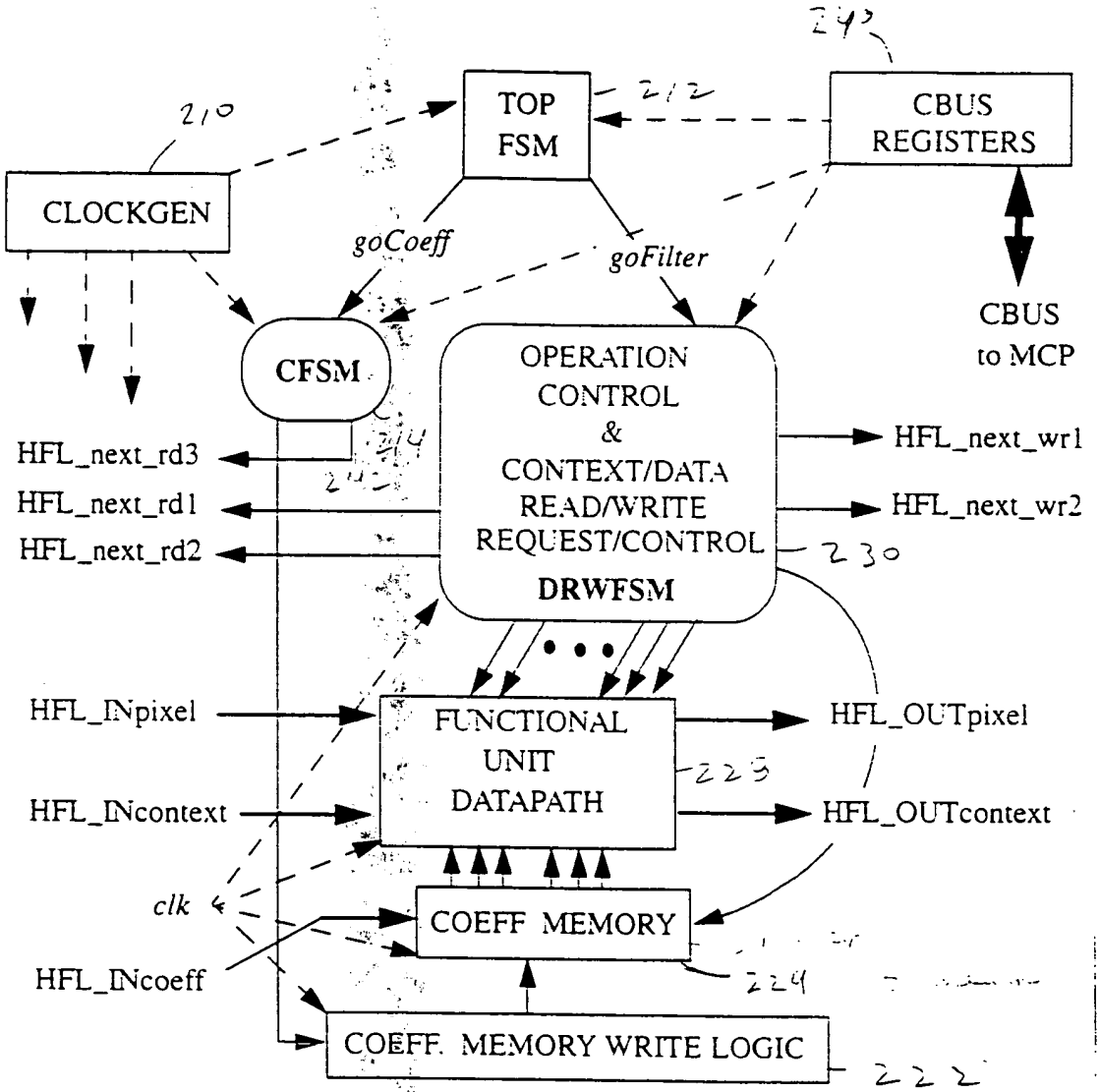

TOP FSM
CBUS REGISTERS
CLOCKGEN
goCoeff
goFilter
CBUS to MCP
CFSM
OPERATION CONTROL & CONTEXT/DATA READ/WRITE REQUEST/CONTROL
DRWFSM
HFL_next_rd3
HFL_next_rd1
HFL_next_rd2
HFL_next_wr1
HFL_next_wr2
HFL_INpixel
HFL_INcontext
FUNCTIONAL UNIT DATAPATH
HFL_OUTpixel
HFL_OUTcontext
clk
COEFF MEMORY
HFL_INcoeff
COEFF. MEMORY WRITE LOGIC

FIG 2

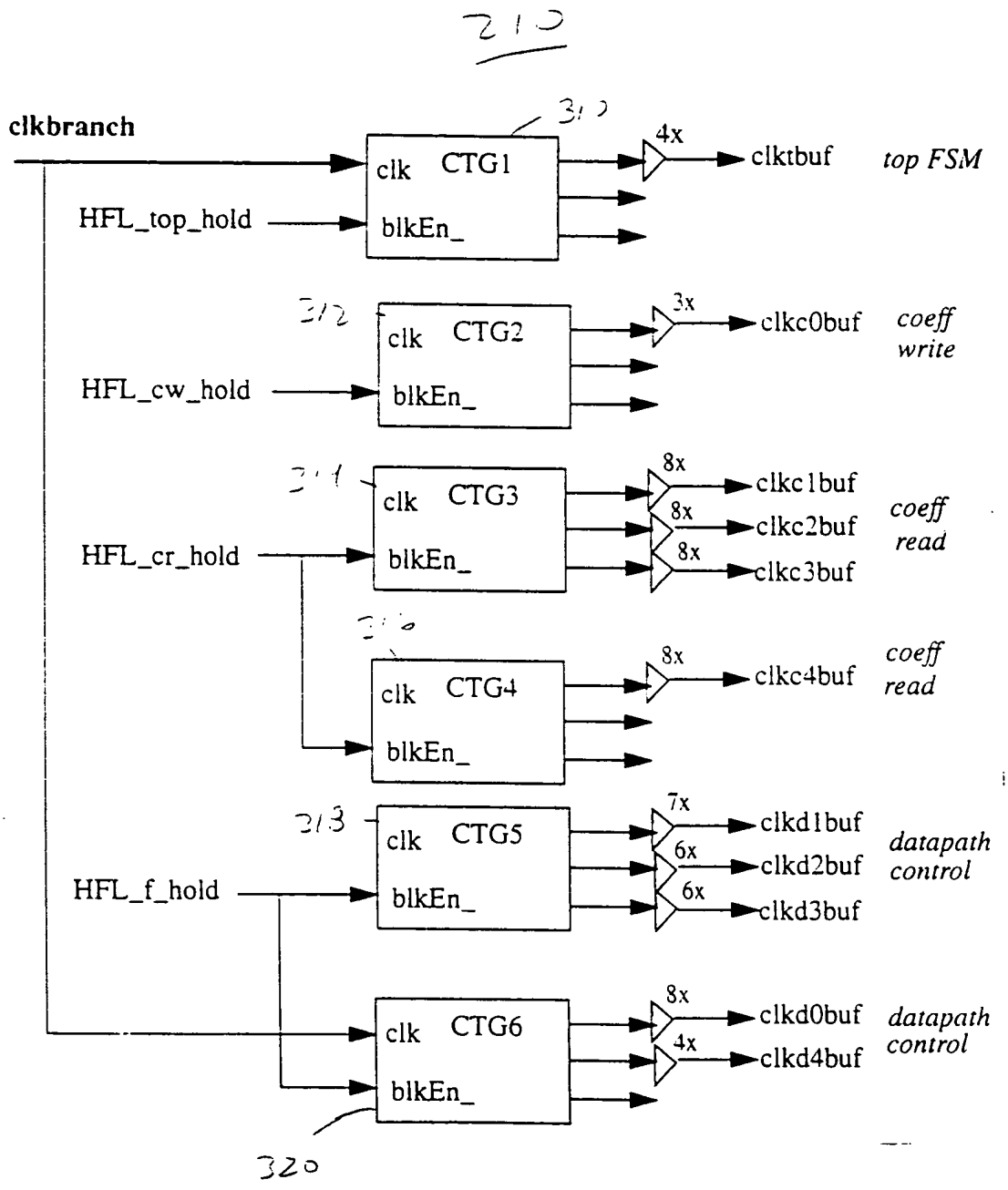
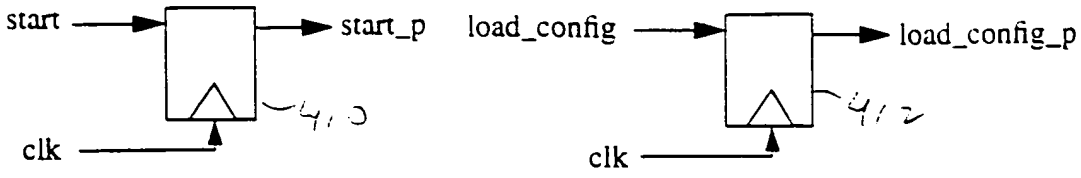

210
clkbranch
310
clk CTG1
blkEn_
HFL_top_hold
4x
clktbuf
top FSM
312
clk CTG2
blkEn_
HFL_cw_hold
3x
clkc0buf
coeff write
311
clk CTG3
blkEn_
HFL_cr_hold
8x
clkc1buf
8x
clkc2buf
8x
clkc3buf
coeff read
316
clk CTG4
blkEn_
8x
clkc4buf
coeff read
313
clk CTG5
blkEn_
HFL_f_hold
7x
clkd1buf
6x
clkd2buf
6x
clkd3buf
datapath control
clk CTG6
blkEn_
8x
clkd0buf
4x
clkd4buf
datapath control
320

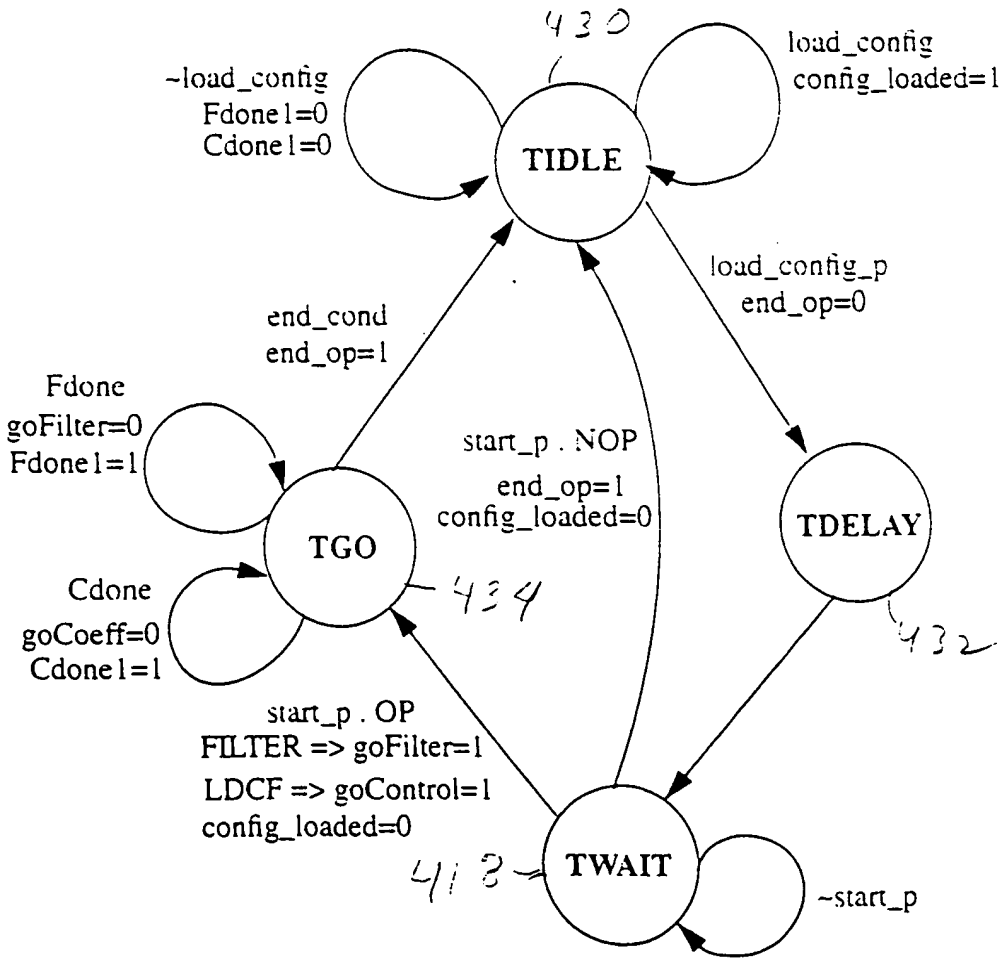
FIG. 3

Fig. 4

212



end_cond= (FILTER && LDCF) ? (Fdone1 && Cdone1)
: ((FILTER) ? Fdone1 : Cdone1)



222

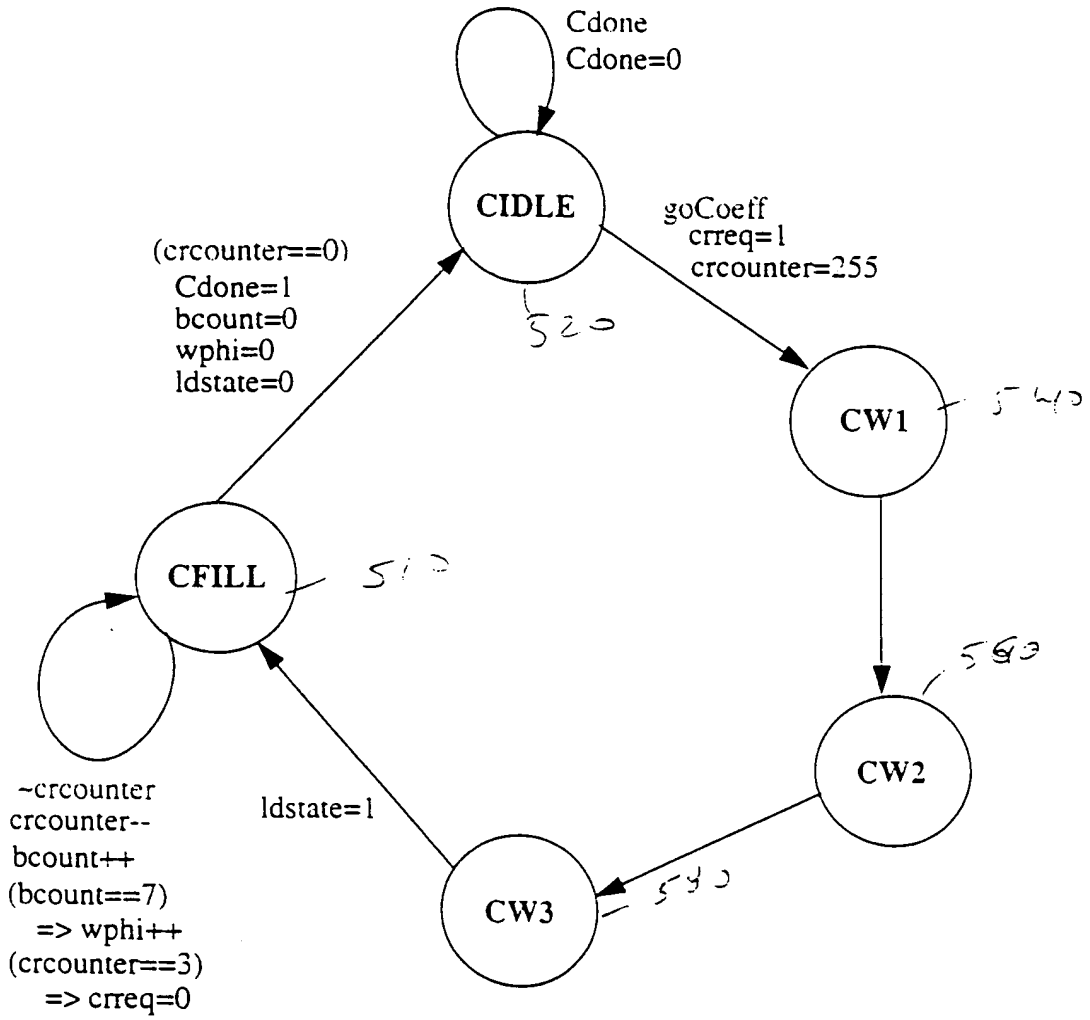

Cdone
Cdone=0
CIDLE
goCoeff
crreq=1
crcounter=255
(crcounter==0)
Cdone=1
bcount=0
wphi=0
ldstate=0
520
CW1
540
CFILL
510
560
CW2
~crcounter
crcounter--
bcount++
(bcount==7)
=> wphi++
(crcounter==3)
=> crreq=0
ldstate=1
CW3
530

FIG. 5

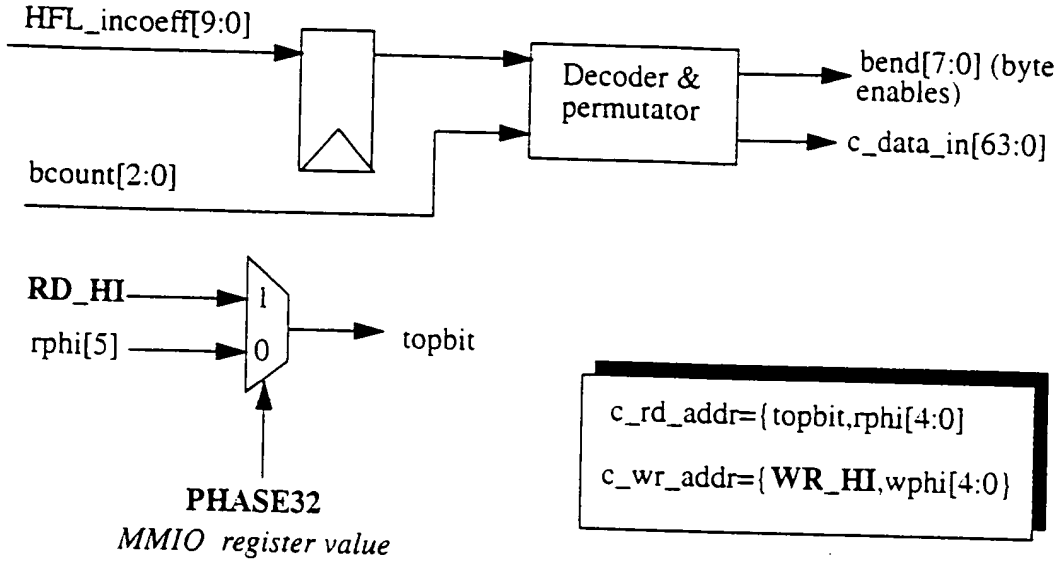

HFL_incoeff[9:0]
Decoder & permutator
bend[7:0] (byte enables)
c_data_in[63:0]
bcount[2:0]
RD_HI
rphi[5]
1
0
topbit
PHASE32
MMIO register value
c_rd_addr={topbit,rphi[4:0]
c_wr_addr={WR_HI,wphi[4:0}

FIG 6A

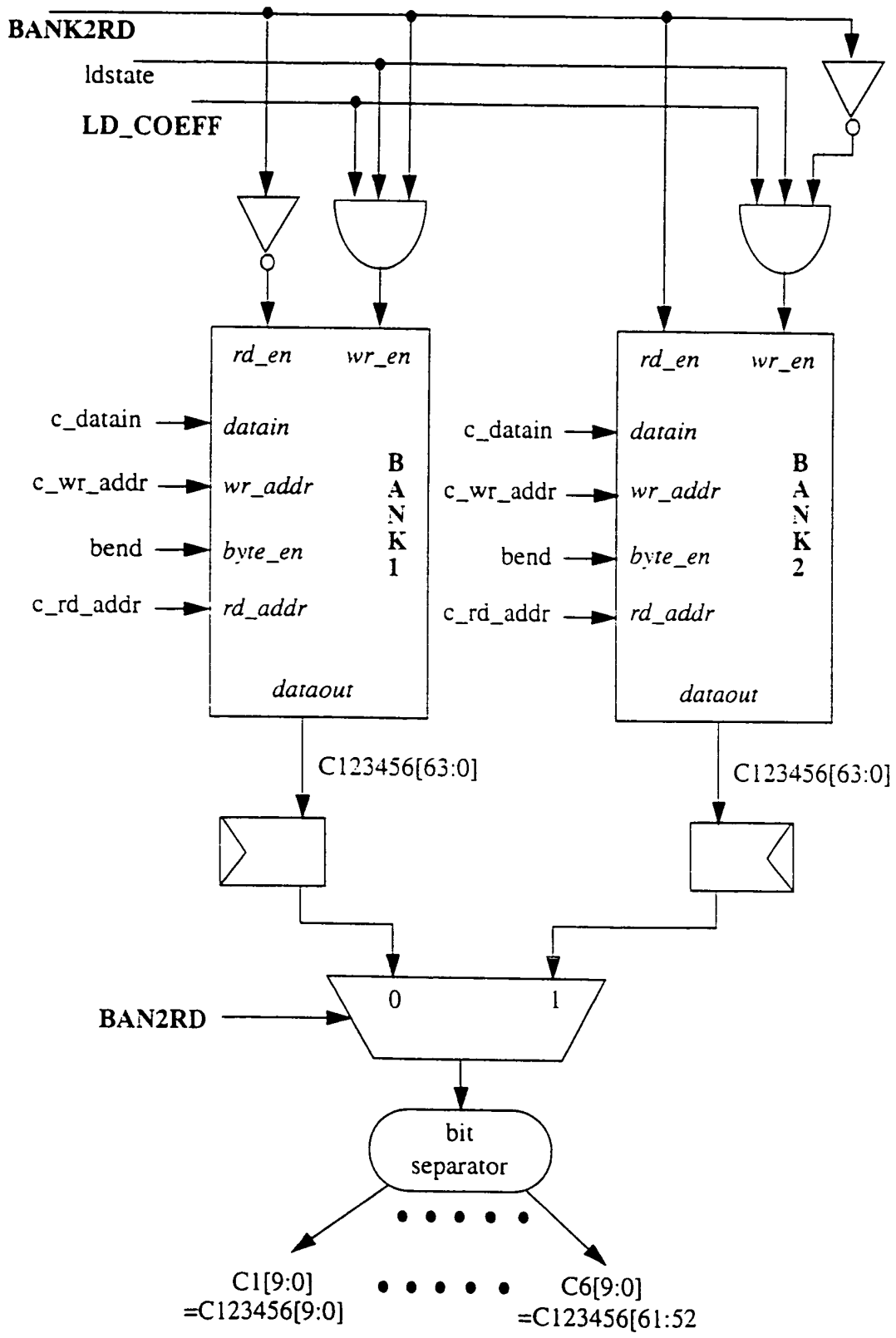

BANK2RD
ldstate
LD_COEFF
rd_en
wr_en
c_datain
datain
c_wr_addr
wr_addr
bend
byte_en
c_rd_addr
rd_addr
dataout
BANK 1
BANK 2
C123456[63:0]
BAN2RD
0
1
bit separator
C1[9:0] =C123456[9:0]
C6[9:0] =C123456[61:52

FIG. 6B

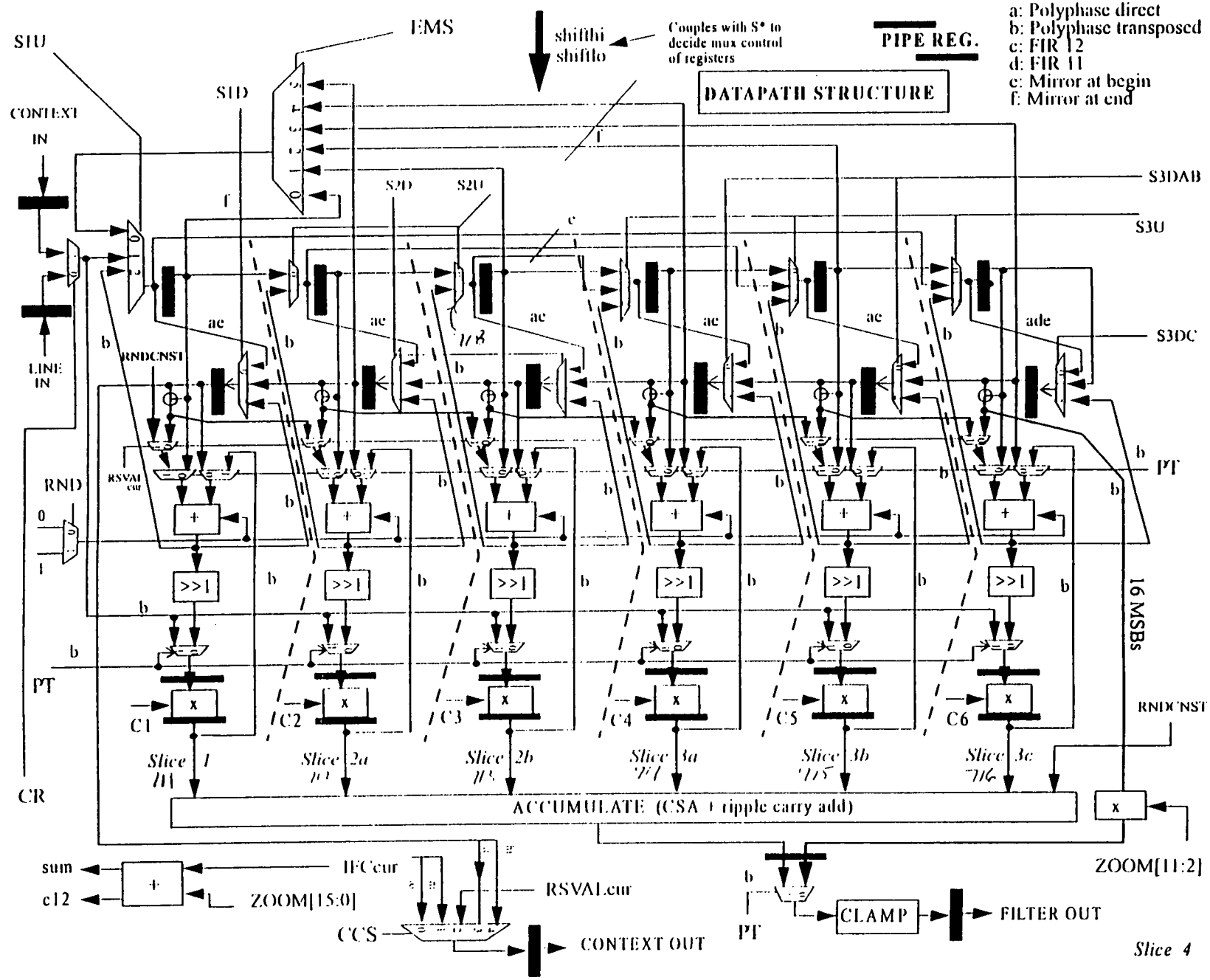

DATAPATH STRUCTURE
PIPE REG.
a: Polyphase direct
b: Polyphase transposed
c: FIR 12
d: FIR 11
e: Mirror at begin
f: Mirror at end
Couples with S* to decide mux control of registers
shiftlhi
shiftlo
EMS
S1U
S1D
CONTEXT IN
LINE IN
S2D
S2U
S3DAB
S3U
S3DC
RNDCNST
RSVAL cur
RND
PT
C1
C2
C3
C4
C5
C6
Slice 1
Slice 2a
Slice 2b
Slice 3a
Slice 3b
Slice 3c
16 MSBs
CR
ACCUMULATE (CSA + ripple carry add)
ZOOM[11:2]
sum
c12
IFC'cur
ZOOM[15:0]
RSVAL cur
CCS
CONTEXT OUT
CLAMP
FILTER OUT
Slice 4

Fig. 7

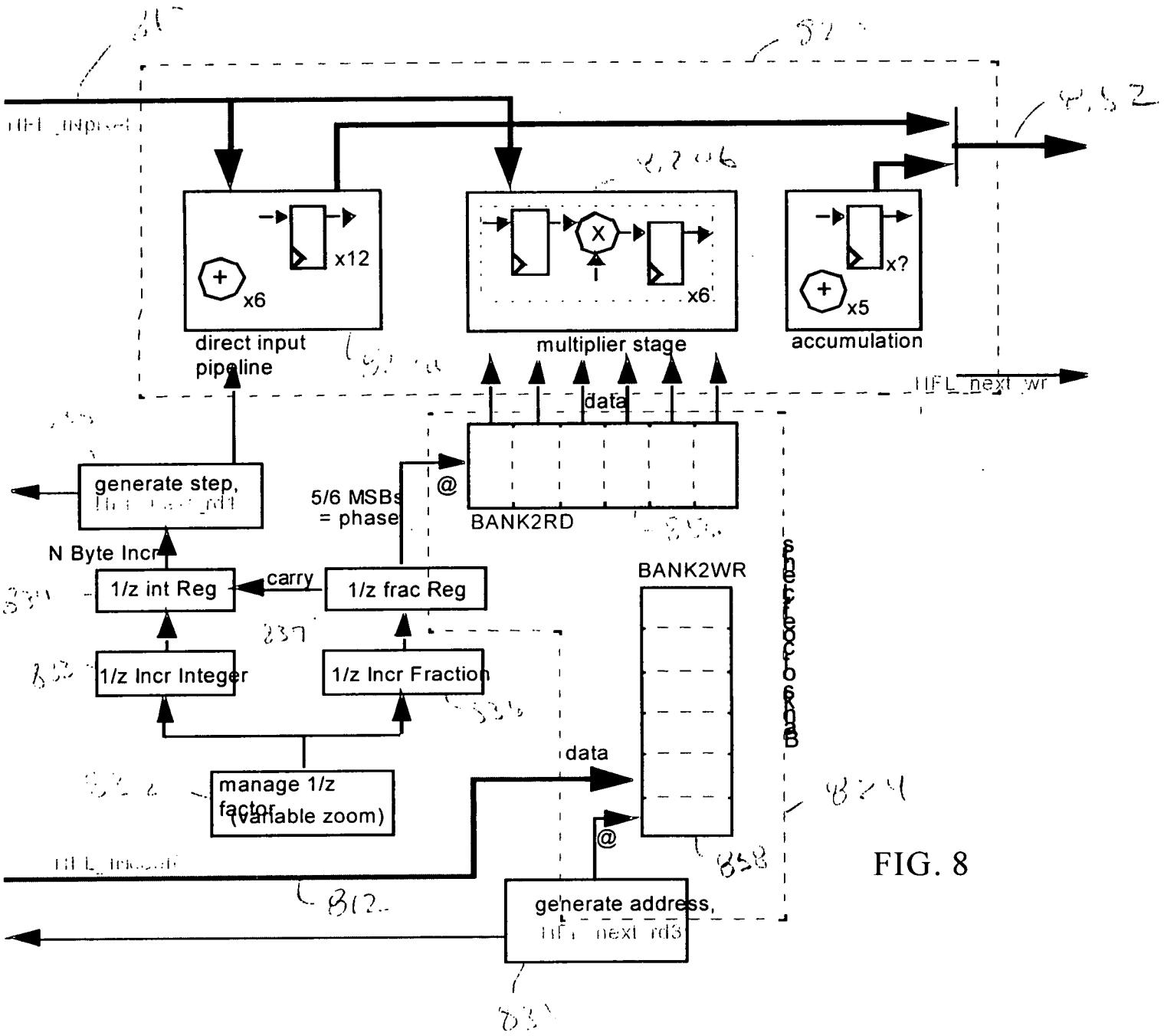


FIG. 8

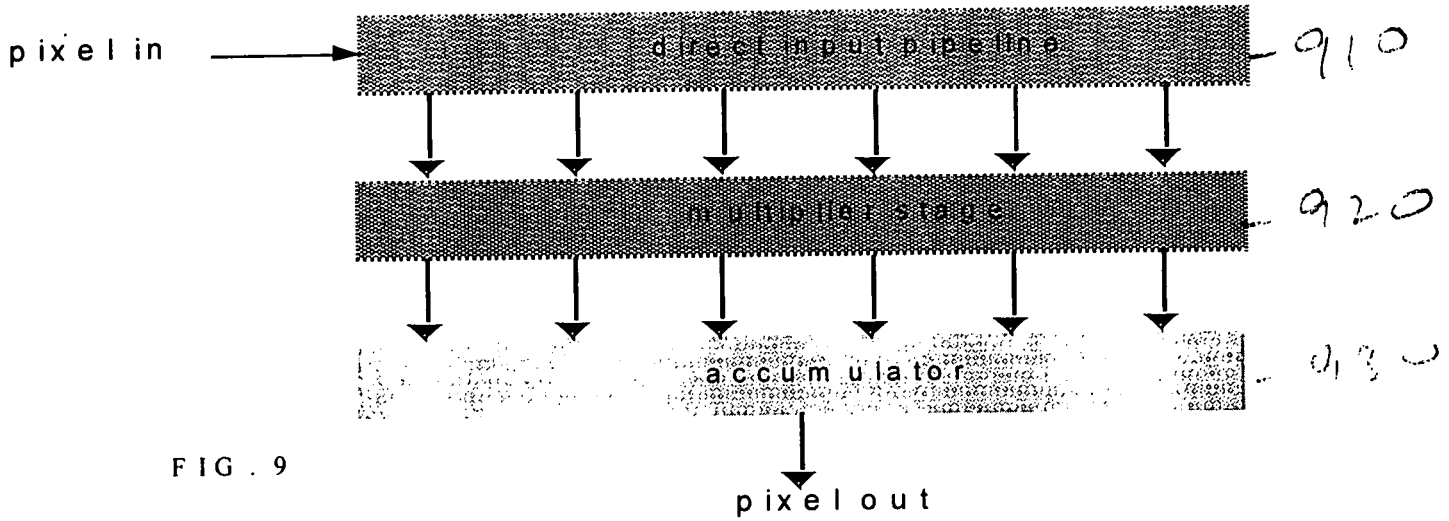
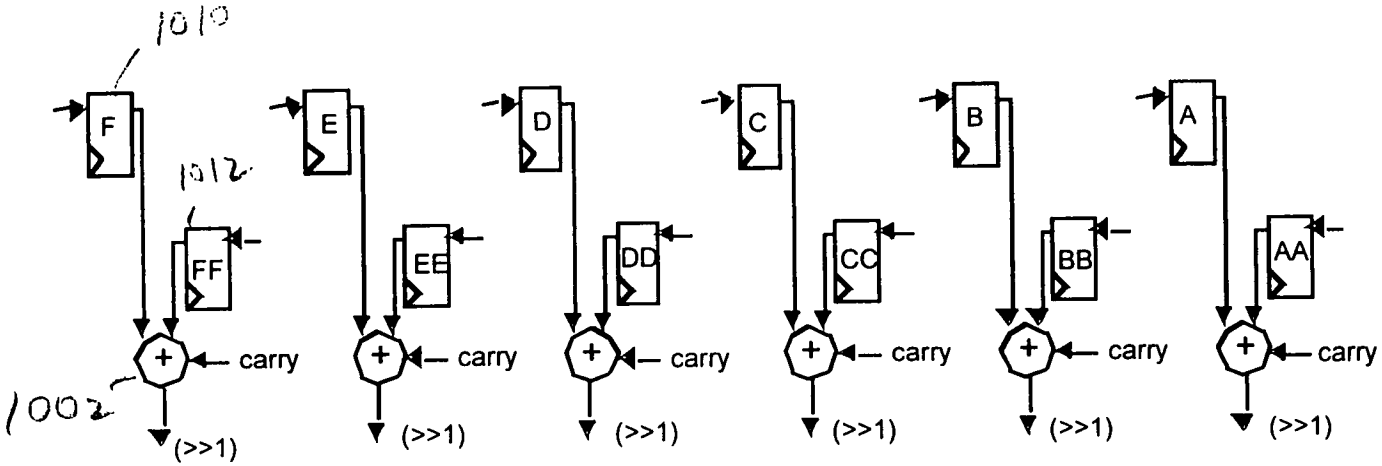

pixel in
direct input pipeline
910
multiplier stage
920
accumulator
930
pixel out

FIG. 9



Direct Input Pipeline

sent to the multiplier stage

FIG. 10

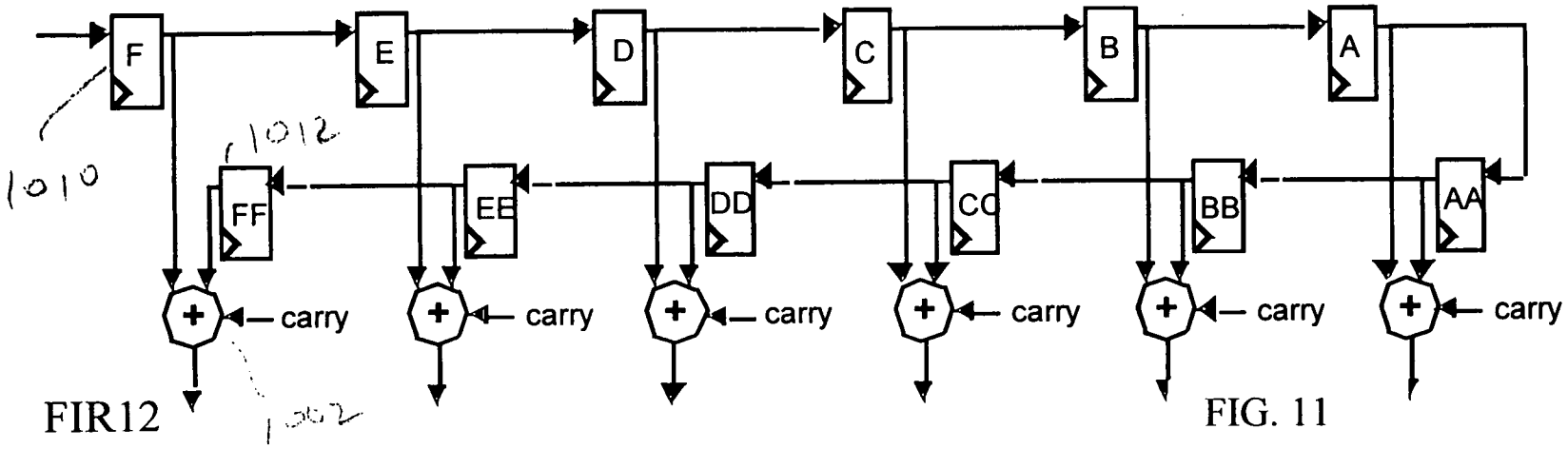
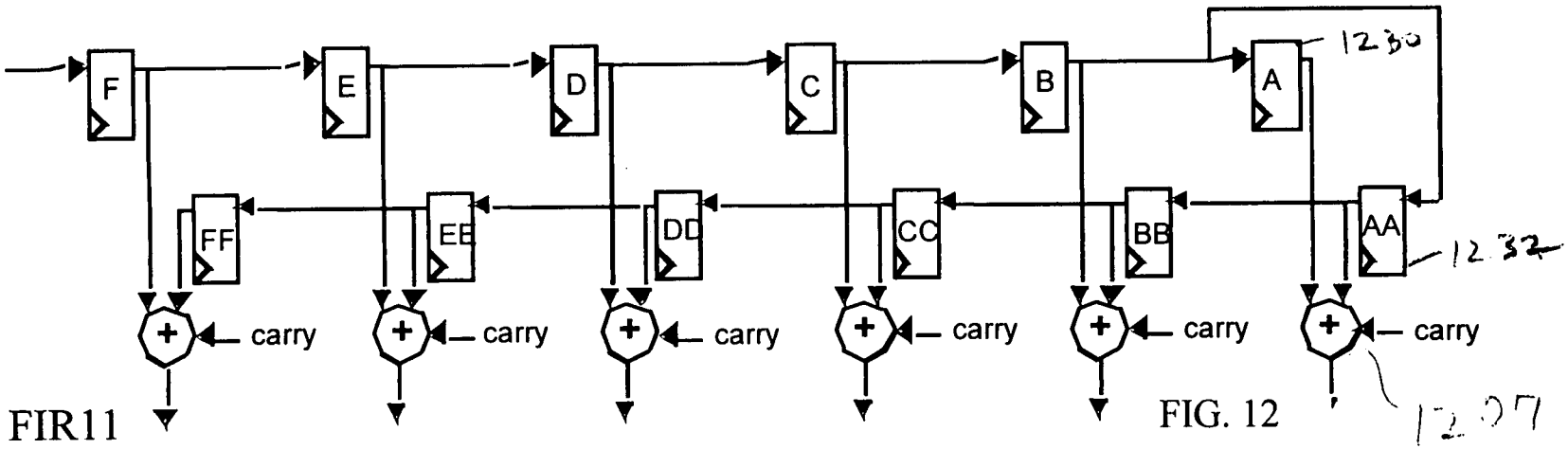
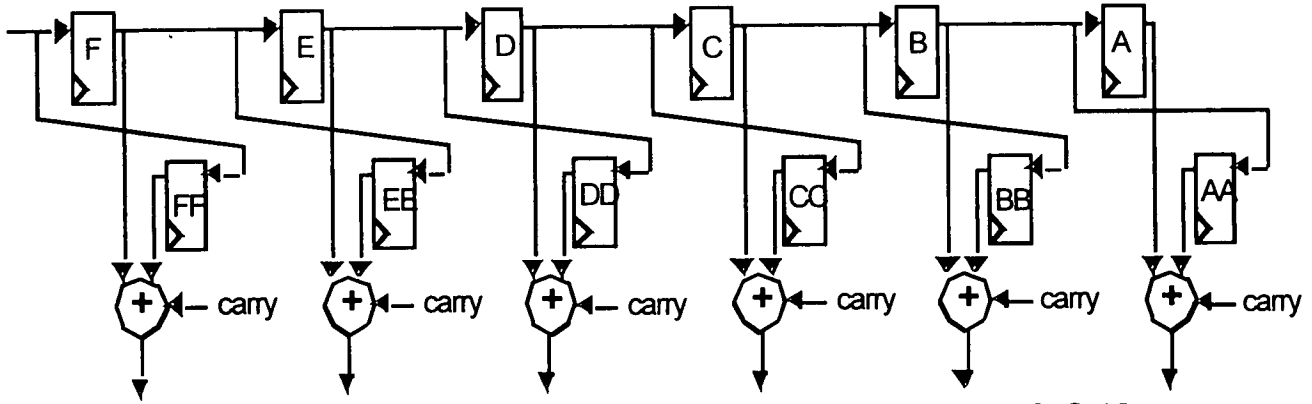


FIG. 11



FIR11

FIG. 12



Polyphase

FIG.13

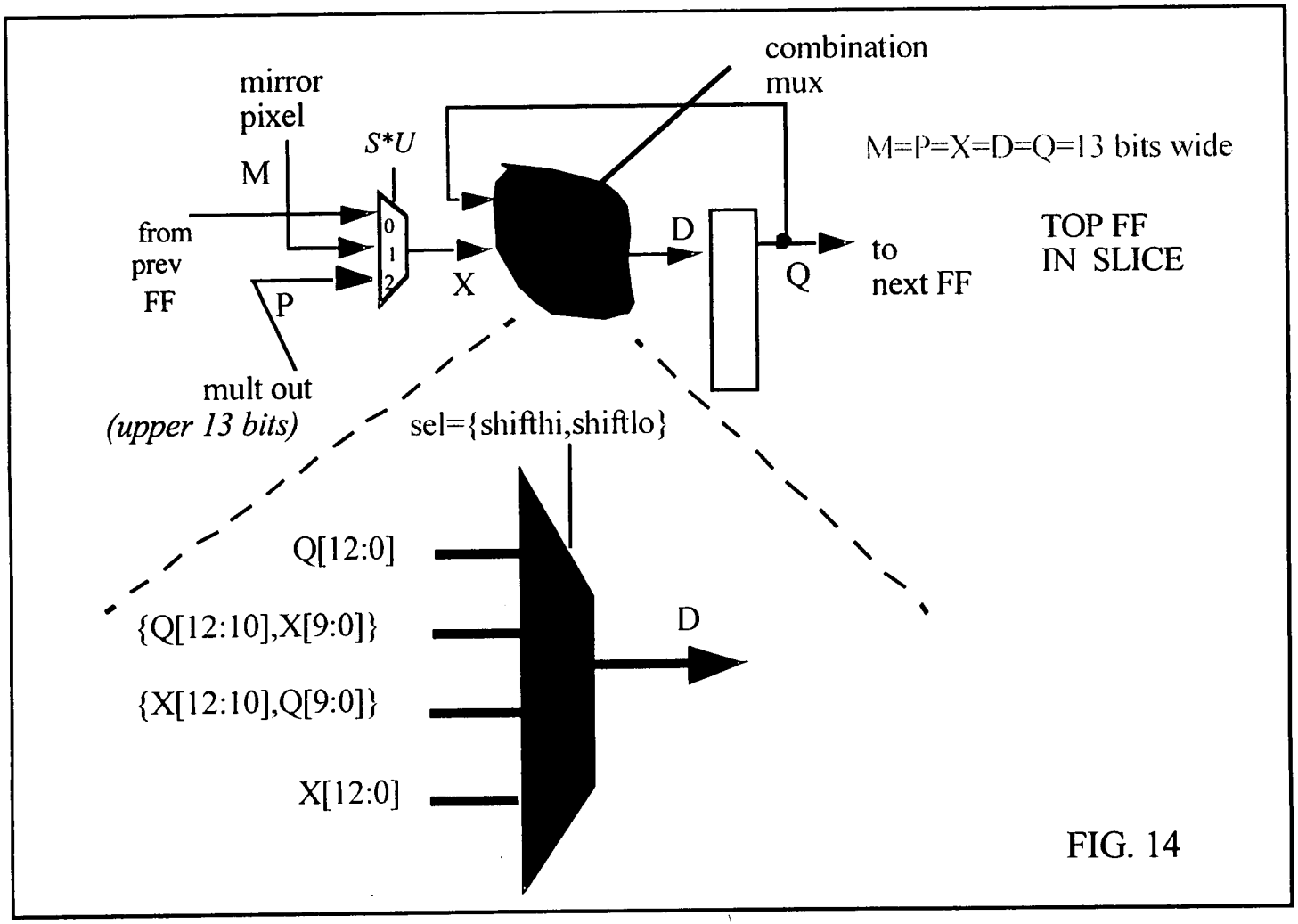

combination
mux
mirror
pixel
S*U
M
M=P=X=D=Q=13 bits wide
from
prev
FF
0
1
2
X
D
Q
to
next FF
TOP FF
IN SLICE
P
mult out
(upper 13 bits)
sel={shifthi,shiftlo}
Q[12:0]
{Q[12:10],X[9:0]}
{X[12:10],Q[9:0]}
X[12:0]
D

FIG. 14

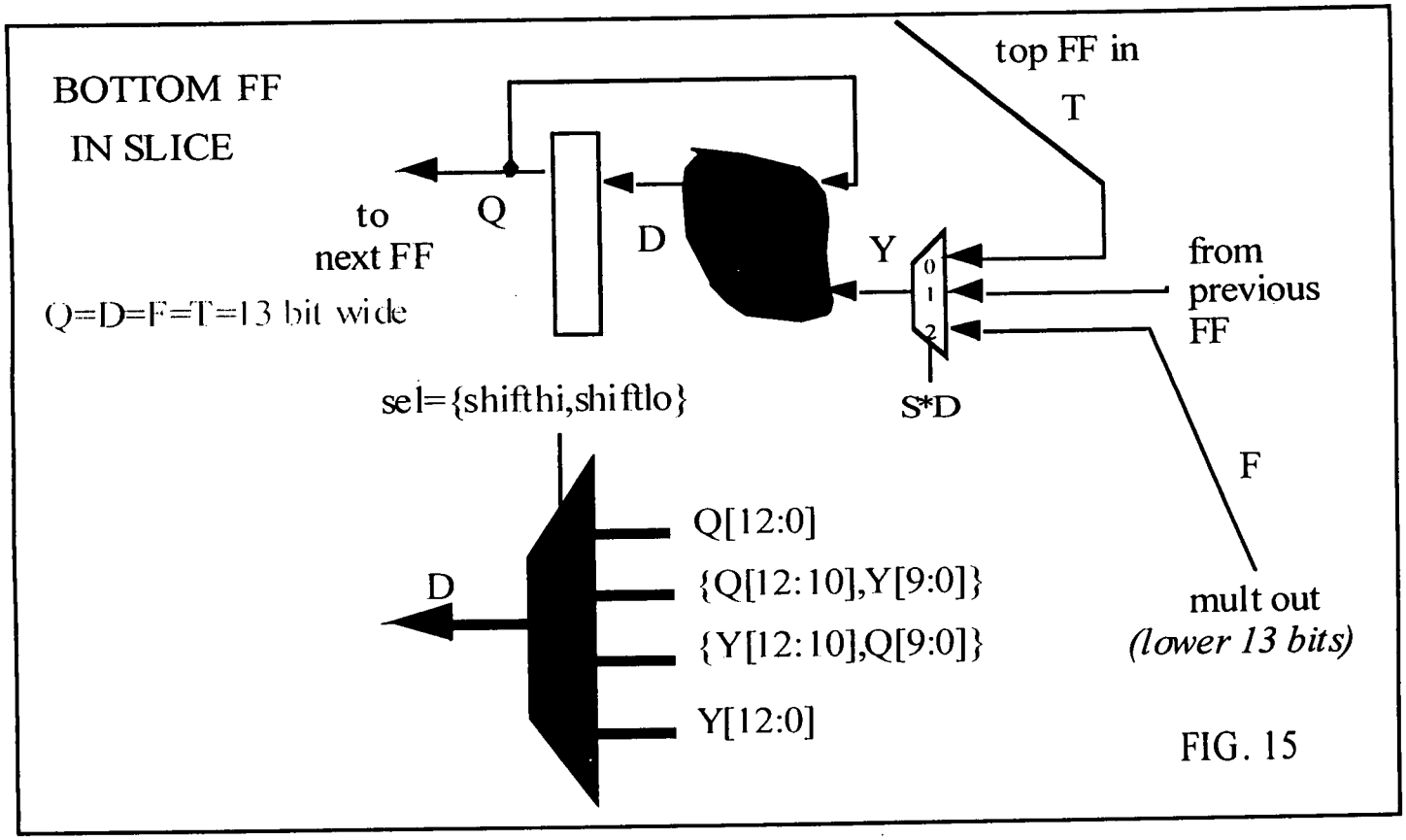

BOTTOM FF
IN SLICE
to
next FF
Q
D
Q=D=F=T=13 bit wide
top FF in
T
Y
0
1
2
from
previous
FF
S*D
F
mult out
(lower 13 bits)
sel={shifthi,shiftlo}
D
Q[12:0]
{Q[12:10],Y[9:0]}
{Y[12:10],Q[9:0]}
Y[12:0]

FIG. 15